



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/329,558	06/10/1999	GRAHAM CHAPMAN	12463(CA998-	8251

7590 06/16/2003

RICHARD L CATANIA ESQ
SCULLY SCOTT MURPHY AND PRESSER
400 GARDEN CITY PLAZA
GARDEN CITY, NY 11530

EXAMINER

TANG, KENNETH

ART UNIT

PAPER NUMBER

2127

DATE MAILED: 06/16/2003

9

Please find below and/or attached an Office communication concerning this application or proceeding.

12

Office Action Summary

Application No.

09/329,558

Applicant(s)

CHAPMAN ET AL.

Examiner

Kenneth Tang

Art Unit

2127

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 May 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 June 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Application 09/329558 was filed on 6/10/99. Claims 1-23 are presented for examination.
2. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "wherein said processing said bytecode sequence is performed without modifying the program bytecodes in the stack" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 1, 11, and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.** The claim(s) contains subject matter which

Art Unit: 2127

was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed subject matter “wherein said processing said bytecode sequence is performed without modifying the program bytecodes in the stack” is not disclosed in the specification..

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-3, 6-7, 9-13, 16-17, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agesen (US 6,047,125) in view of Gosling (US 5,668,999).

Referring to claims 1 and 11, Agesen teaches the following limitations:

- simulating stack actions for executing bytecodes along said path (“bytecode”, “stack”, “execution”, col 3, lines 62-65, and “pushed on stack by bytecode”, “execution”, col 11, lines 59-63);
- mapping a path of control flow on the stack from any start point in a selected method to the destination program counter by locating a linear path from the beginning of the

Art Unit: 2127

method to the destination program counter and iteratively processing a bytecode sequence for each branch until said destination program counter is reached.

Agesen discloses using a stack mapping (*"stack map", "mapped to the same slot in the stack frame", col. 3, lines 13-47*). It is inherent that all computer systems, including Agesen's computer system, have a control processor (CPU) that controls the flow of every other units, thus being known as the "brain of the computer." It is also inherent to one of ordinary skill in the art that a processor (CPU) maintains a register known as the *program counter*. A program counter holds the address of the current instruction. After an instruction completes, the processor automatically and iteratively adds one to the program counter until computing instructions tell it to stop. That's what a program counter does.

Agesen fails to explicitly teach:

- constructing a virtual stack for storage in a pre-allocated memory location

However, Gosling discloses generating a "virtual stack" 344 from the step of simulating stack actions executing "bytecodes" in memory (col 5, lines 21-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the virtual stack feature to the existing system of Agesen for the reason of being able to have an imaginary stack to store bytecodes.

Agesen also fails to explicitly teach:

- wherein said processing said bytecode sequence is performed without modifying the program bytecodes in the stack.

However, Gosling's system and method also teaches no modification of bytecode (*"no instructions for modifying object references", "ensure that any bytecode program which utilizes*

Art Unit: 2127

data in a manner consistent with the data” will “not violate the integrity of a user’s computer system”, col. 3, lines 33-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of not modifying the bytecode for the reason of “improving the integrity of a user’s computer system” by ensuring that the bytecode is handled in a consistent manner (*col. 3, lines 40-48*).

Referring to claims 2 –3, and 12-13, Agesen teaches:

- processing a first linear bytecode sequence and an additional one until the control flow is interrupted (“two or more bytecode sequences”, col 5, lines 19-27, and “Interrupt controller”, Fig. 3A 135, col 7, lines 42-44)
- recording unprocessed targets from any branches in the first and additional linear bytecode sequence for future processing (Exception handler 760, bytecode 732, “stores a reference in variable 1”, “branch to bytecode”, col 11, lines 54-59).

Ageson inherently teaches:

- the destination program counter was not reached during an earlier processing of a linear bytecode sequence
- the information stored in the reference can be used at a future time for processing.

Ageson does teach that the program counter was reached during the later processing of a bytecode sequence (The bytecode 740 is stored in variable 2 value of the program counter, col 11, lines 45-47). In Ageson’s reference, the program counter does not get reached in the earlier processing.

Art Unit: 2127

Referring to claims 6 and 16, Agesen fails to explicitly teach generating a virtual stack from executing bytecodes along the path. However, Gosling discloses generating a “virtual stack” 344 from the step of simulating stack actions executing “bytecodes” (col 5, lines 21-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the virtual stack feature to the existing system of Agesen for the reason of being able to have an imaginary stack to store bytecodes.

Referring to claims 7 and 17, Gosling discloses:

- storing the bitstring at a selected destination for use in memory management operations (virtual stack 344 stored by bytecode, col 5, lines 33-40).

Gosling does not disclose:

- encoding the virtual stack as a bitstring

However, it is common knowledge that bitstrings can be encoded from binary.

Referring to claims 9 and 19, Agesen teaches storing the bitstring to a pre-allocated area on the stack (“bytecode 704 stores the value (1) from the top of the operand stack”, col 11, lines 5-12).

Referring to claims 10 and 20, Agesen teaches inserting pre-determined stack actions for bytecodes maintaining the control flow (“Bytecode 702 is used to push the integer value 1 on top of the operand stack”, col 11, lines 5-6) and calculating stack actions for bytecodes transferring the control flow (bytecodes, stack, $i=i+itmp$, col 11, lines 19-23).

Art Unit: 2127

Referring to claims 21 and 22, it is inherent that computer-readable memory can be used to store instructions.

Referring to claims 23, it is rejected for the same reasons as stated in the rejections of claims 1-3.

6. Claims 4-5, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agesen (US 6,047,125) in view of Agesen (US 5,909,579).

Referring to claims 4-5 and 14-15, Agesen (US 6,047,125) fails to explicitly teach:

- determining if a bytecode in any linear bytecode sequence is a breakpoint with a pointer to bytecode data;

However Agesen (US 5,909,579) teaches a “bytecode analyzer mechanism” which determines the changes which the bytecode makes to the live pointer locations (col 8, lines 20-24). In addition, the system has breakpoints or computation stops at bytecode boundaries for determining live pointer information (col 3, lines 10-13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the determination of a breakpoint feature to the existing system of Agesen for the reason of improving control by having an interrupt mechanism.

Agesen (US 6,047,125) also fails to explicitly teach:

- replacing the breakpoint with the bytecode data

Art Unit: 2127

However Ageson (US 5,909,579) also teaches an encoded bytecode change to the breakpoint or program stack frame pointer (bytecode encoded, change, program stack frame live pointer, col 8, lines 25-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of replacing the breakpoint with the bytecode data for the reason of giving the system more flexibility for optimizing garbage collection.

7. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Agesen (US 6,047,125) in view of Gosling (US 5,668,999) and further in view of O'Connor (US 6,098,089).

Referring to claims 8 and 18, Agesen in view of Gosling fails to explicitly teach storing the bitstring on a heap. However, from the reference of O'Connor, it is well-known in the state of the art that "garbage collection" of "heap-allocated storage" is an "attractive model for dynamic memory management" (col 1, lines 39-42). It is known that dynamic refers to actions that take place when they are needed (compile time) rather than in advance. For example, many programs perform *dynamic memory allocation*, which means that they do not reserve memory ahead of time, but seize sections of memory when needed. In general, such programs require less memory, although they may run a little more slowly.

Art Unit: 2127

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (703) 305-5334. The examiner can normally be reached on 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (703)305-8498. The fax phone numbers for the organization where this application or proceeding is assigned are none for regular communications and none for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is none.

kt
June 8, 2003


MAJID A. BANANKHAH
PRIMARY EXAMINER